What is claimed is:

1. An MPEG data processing circuit which processes inputted MPEG data to produce outputted MPEG data, comprising:

dividing means which divide said inputted MPEG data into a first data block having a plurality of first data to be processed and a second data block having a plurality of second data to be not processed;

primary storing means which store said a plurality of first data to be processed;

secondary storing means which store the numbers of said first data stored in said primary storing means or said a plurality of second data to be not processed;

primary extracting and partially replacing means which extract said a plurality of first data to be processed from said primary storing means in accordance with an order of said inputted MPEG data and which partially replace a predetermined data portion of the extracted first data; said primary extracting and partially replacing means producing a primary data block;

secondary extracting means which extract said a plurality of second data to be not processed from said secondary storing means in accordance with an order of said inputted MPEG data to produce a secondary data block; and

combining means which combine said primary data

block and said secondary data block with each other in an original order to produce said outputted MPEG data.

2. An MPEG data processing circuit which processes inputted MPEG data to produce outputted MPEG data, comprising:

V-ES detecting section which judges said inputted MPEG data to output video stream status signal indicating output status of system stream data and video elementary data within said system stream data;

a memory which stores non-video elementary data portion from said V-ES detecting section;

a barrel shifter which divides video elementary data portion from said V-ES detecting section into bit units and which stores the bit units of said video elementary data portion;

a variable length decoder which is connected to an output of said barrel shifter;

a data replacing section which is connected to an output of said variable length decoder;

a variable length encoder which is connected to an output of said data replacing section;

a bit packer section which is connected to an output of said variable length encoder;

a data combining section which combines an output of said bit packer section and an output of said memory to produce said outputted MPEG data in an original order;

a control section which controls input and output of

data in said barrel shifter and said data replacing section based on a first control signal from said V-ES detecting section, a signal from said variable length decoder, and a signal from said data combining section; and

a memory control section which controls input and output of data in said memory based on said first control signal from said V-ES detecting section and which outputs a second control signal to said control section.

3. An MPEG data processing circuit as claimed in claim 2, wherein said memory control section refers an amount of remaining data in said memory in a case that not fewer than one byte of video data stream are outputted from said V-ES detecting section, said memory control section making data in said barrel shifter be outputted from said data combining section when no data are stored in said memory.

4. An MPEG data processing circuit as claimed in claim 2, wherein said data replacing section is an electronic watermark inserting section, said MPEG data processing circuit further comprising an electronic watermark detecting section which is connected to an output of said variable length decoder.

5. An MPEG data processing circuit as claimed in claim 3, wherein said data replacing section is an electronic watermark inserting section, said MPEG data processing

circuit further comprising an electronic watermark detecting section which is connected to an output of said variable length decoder.

6. An MPEG data processing circuit as claimed in claim 2, further comprising:

a preceding output length storing section for storing numbers of remaining data stored in said barrel shifter to be precedingly outputted therefrom with the numbers of remaining data being kept therein; and

a fraction length storing section for storing difference obtained by subtracting a stored value in said preceding output length storing section from numbers of data outputted in response to data, at first, inputted to said barrel shifter after the preceding output.

7. An MPEG data processing circuit as claimed in claim 3, further comprising:

a preceding output length storing section for storing numbers of remaining data stored in said barrel shifter to be precedingly outputted therefrom with the numbers of remaining data being kept therein; and

a fraction length storing section for storing difference obtained by subtracting a stored value in said preceding output length storing section from numbers of data outputted in response to data, at first, inputted to said barrel shifter after the preceding output.

8. An MPEG data processing circuit as claimed in claim 4, further comprising:

a preceding output length storing section for storing numbers of remaining data stored in said barrel shifter to be precedingly outputted therefrom with the numbers of remaining data being kept therein; and

a fraction length storing section for storing difference obtained by subtracting a stored value in said preceding output length storing section from numbers of data outputted in response to data, at first, inputted to said barrel shifter after the preceding output.

9. A method of controlling an MPEG data processing circuit, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into a first data block to be processed and a second data block to be not processed;

primary storing said first data block to be processed in a primary storing section;

secondary storing said second data block to be not processed in a secondary storing section;

replacing a value of a predetermined position of data group obtained by variable length decoding said first data block to be processed stored in said primary storing section with a desired value;

obtaining a processed data block by variable length encoding the replaced data group; and

combining said processed data block and said second

data block to be not processed stored in said secondary storing section with each other in an order of input to be outputted as an MPEG data stream.

10. A method of controlling an MPEG data processing circuit as claimed in claim 9, further comprising the steps of:

referring an amount of remaining data in said secondary storing section; and

writing data in said secondary storing section without waiting for an input of data to be replaced, when no data are stored therein.

11. A method of controlling an MPEG data processing circuit for use in controlling said MPEG data processing circuit as claimed in claim 8, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into non-video elementary data portion and video elementary data portion;

primary storing said non-video elementary data portion in said memory;

secondary storing said video elementary data portion in said barrel shifter;

replacing a value of a predetermined position of data group obtained by variable length decoding said video elementary data portion stored in said barrel shifter with a desired value;

obtaining a processed data block by variable length encoding the replaced data group;

combining said processed data block and said non-video elementary data portion stored in said memory with each other in an order of input to be outputted as an MPEG data stream; and

storing numbers of remaining data stored in said barrel shifter in said preceding output length storing section and outputting the numbers of remaining data from said barrel shifter with the remaining data being kept therein, when it is detected that said memory is full, that said data combining section is condition waiting for an input, that all of said variable length decoder, said electronic watermark inserting section, and said variable length encoder have no data, that said barrel shifter has remaining data, and that the remaining data cannot be decoded.

12. A method of controlling an MPEG data processing circuit for use in controlling said MPEG data processing circuit as claimed in claim 8, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into non-video elementary data portion and video elementary data portion;

primary storing said non-video elementary data portion in said memory;

secondary storing said video elementary data portion

in said barrel shifter;

replacing a value of a predetermined position of data group obtained by variable length decoding said video elementary data portion stored in said barrel shifter with a desired value;

obtaining a processed data block by variable length encoding the replaced data group;

combining said processed data block and said non-video elementary data portion stored in said memory with each other in an order of input to be outputted as an MPEG data stream; and

controlling said barrel shifter, in a case that said barrel shifter has remaining data, to output the remaining data therefrom, when it is detected that said MPEG data stream is not inputted for a certain time.

13. A method of controlling an MPEG data processing circuit for use in controlling said MPEG data processing circuit as claimed in claim 8, said method comprising the steps of:

dividing an MPEG data stream inputted to said MPEG data processing circuit into non-video elementary data portion and video elementary data portion;

primary storing said non-video elementary data portion in said memory;

secondary storing said video elementary data portion in said barrel shifter;

replacing a value of a predetermined position of data

group obtained by variable length decoding said video elementary data portion stored in said barrel shifter with a desired value;

obtaining a processed data block by variable length encoding the replaced data group;

combining said processed data block and said non-video elementary data portion stored in said memory with each other in an order of input to be outputted as an MPEG data stream; and

controlling said barrel shifter, in a case that said barrel shifter has remaining data, to output the remaining data therefrom, when a notice of finish of input of a unit of said MPEG data stream is inputted from the outside of said MPEG data processing circuit.